Allwinner F1C500

Datasheet

V1.0

2014-5-28

Declaration

THIS F1C500 DATASHEET IS THE ORIGINAL WORK AND COPYRIGHTED PROPERTY OF ALLWINNER TECHNOLOGY ("ALLWINNER"). REPRODUCTION IN WHOLE OR IN PART MUST OBTAIN THE WRITTEN APPROVAL OF ALLWINNER AND GIVE CLEAR ACKNOWLEDGEMENT TO THE COPYRIGHT OWNER.

THE INFORMATION FURNISHED BY ALLWINNER IS BELIEVED TO BE ACCURATE AND RELIABLE. ALLWINNER RESERVES THE RIGHT TO MAKE CHANGES IN CIRCUIT DESIGN AND/OR SPECIFICATIONS AT ANY TIME WITHOUT NOTICE. ALLWINNER DOES NOT ASSUME ANY RESPONSIBILITY AND LIABILITY FOR ITS USE. NOR FOR ANY INFRINGEMENTS OF PATENTS OR OTHER RIGHTS OF THE THIRD PARTIES WHICH MAY RESULT FROM ITS USE. NO LICENSE IS GRANTED BY IMPLICATION OR OTHERWISE UNDER ANY PATENT OR PATENT RIGHTS OF ALLWINNER. THIS DATASHEET NEITHER STATES NOR IMPLIES WARRANTY OF ANY KIND, INCLUDING FITNESS FOR ANY PARTICULAR APPLICATION.

THIRD PARTY LICENCES MAY BE REQUIRED TO IMPLEMENT THE SOLUTION/PRODUCT. CUSTOMERS SHALL BE SOLELY RESPONSIBLE TO OBTAIN ALL APPROPRIATELY REQUIRED THIRD PARTY LICENCES. ALLWINNER SHALL NOT BE LIABLE FOR ANY LICENCE FEE OR ROYALTY DUE IN RESPECT OF ANY REQUIRED THIRD PARTY LICENCE. ALLWINNER SHALL HAVE NO WARRANTY, INDEMNITY OR OTHER OBLIGATIONS WITH RESPECT TO MATTERS COVERED UNDER ANY REQUIRED THIRD PARTY LICENCE.

Revision History

Revision	Date	Description
V1.0	2014-5-28	

Table of Contents

1.Overview

The F1C500 processor is a highly integrated programmable platform for multimedia devices. The F1C500 processor contains a rich set of peripherals connected to the ARM9 CPU via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance.

The general-purpose peripherals include functions such as USB HS/FS DRD, UART, SPI, TWI, RSB, CMOS Sensor I/F, LCD controller, TV encoder, TV decoder, SD/MMC I/F, SDRAM/DDR I/F. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the part. In addition to these general-purpose peripherals, the F1C500 processor contains high speed serial and parallel ports for interfacing to a variety of audio and video function.

2. Features

2.1. CPU Architecture

The F1C500 platform is based on ARM9 CPU architecture.

- Five-stage pipeline architecture
- Support 16KByte D-Cache
- Support 32KByte I-Cache

2.2. Memory Subsystem

This section consists of:

- Boot ROM
- SDRAM
- SD/MMC interface

Boot ROM

- On-Chip ROM boot loader
- Support system boot from SPI Nor/Nand Flash, and SD/TF card
- Support system code download through USB DRD

SDRAM

- Support SDR SDRAM and DDR SDRAM
- Support different memory device's power voltage of 2.5V and 3.3V
- Thirteen address lines and two bank address lines
- Data IO size is 16-bit for SDR/ DDR
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Clock frequency can be chosen for different application
- Random read or write operation is supported

SD/MMC Interface

- Support secure digital memory protocol commands (up to SD2.0)
- Support secure digital I/O protocol commands (up to SDIO2.0)
- Support multimedia card protocol commands (up to eMMC4.41)
- Support CE-ATA digital protocol commands
- Support eMMC boot operation and alternative boot operation
- Support command completion signal and interrupt to host processor and command completion signal disable feature
- Support one SD (Verson1.0 to 2.0) or MMC (version 3.3 to eMMC4.41) or CE-ATA device
- Support hardware CRC generation and error detection
- Support programmable baud rate
- Support host pull-up control
- Support SDIO interrupts in 1-bit and 4-bit modes
- Support SDIO suspend and resume operation
- Support SDIO read wait
- Support block size of 1 to 65535 bytes
- Support descriptor-based internal DMA controller
- Internal 128 bytes FIFO for data transfer
- Support 3.3V IO pad

2.3. System Peripheral

This section includes:

- Timer
- INTC
- CCM
- DMA
- PWM

Timer

- Three timers
- Support watchdog reset
- Support audio and video synchronize counter

INTC

- Support up to 64 interrupts
- Support 4-level priority
- Support interrupt mask
- Support interrupt fast forcing
- Support one external interrupt

CCM

- Support 6 PLLs
- Control of clock generation, division, distribution and gating
- Control of device software reset

DMA

- Support Normal DMA and Dedicated DMA
- Support two kinds of interrupt
- Support hardware continuous transfer mode

PWM

- Support two PWM outputs
- Support cycle mode and pulse mode
- Support 24MHz maximum output frequency

2.4. Display Subsystem

Display Engine

- Support four layers overlay, each layer size up to 2048x2048 pixels
- Support Alpha blending / color key
- Support multi-format input formats
  - 1/2/4/8/16/32 bpp color
  - YUV444/YUV422/YUV420/YUV411
- Support hardware cursor
- Support scaling function for one layer
  - ARGB8888/YUV444/YUV420/YUV422/YUV411
  - Input and output size up to 1280x720 pixels
  - Resize ratio from 1/16X to 32X
  - 4-tap 32-phase anti-aliasing filter in horizontal and vertical direction
  - Scaler supports write-back to memory function

Display Output

- LCD RGB interface, TTL interface, up to 1280x720@60fps
- LCD Serial RGB interface, CCIR656 interface, up to 720x576@60fps
- LCD i8080 interface with 18/16/9/8 bit, up to 800x480@60fps
- LCD Dither function, support RGB666/RGB565 interface
- TV CVBS output, support NTSC/PAL, with auto plug detecting

CVBS Input

- Support NTSC/PAL
- Support 3D comb filter
- Support two switchable channels

2.5. Video Engine

- Support H.264 BP/MP/HP up to 1920x1080@30fps decoding
- Support format Mpeg1 and Mpeg2 up to 1920x1080@30fps decoding
- Support format Mpeg4 SP/ASP GMC and H.263 including Sorenson Spark up to 1920x1080@30fps decoding
- Support MJPEG encode up to 1280x720@30fps
- Support JPEG encode size up to 8192 x 8192
- Support JPEG decode size up to 16384 x 16384

2.6. Image Subsystem

CSI

- Support 8-bit CMOS-sensor interface
- Support YUV camera up to 5Mega pixel
- Support CCIR656 protocol for NTSC and PAL

2.7. Audio Subsystem

Audio Codec

- Two audio digital-to-analog(DAC) channels
- Stereo capless headphone drivers:
  - Up to 100dB DR
  - Supports DAC Sample Rates from 8KHz to 192KHz
- Support analog/ digital volume control
- Analog low-power loop from FM/ line-in /microphone to headphone outputs
- Four audio inputs:
  - One microphone input
  - Stereo FM input
  - One Line-in input
- One audio analog-to-digital(ADC) channel
  - 96dBA SNR
  - Supports ADC Sample Rates from 8KHz to 48KHz
  - Support AGC (Auto Gain Control)

2.8. System Peripherals

This section includes:

- USB2.0 DRD

- KEYADC
- TP
- Digital Audio Interface
- UART
- SPI
- TWI
- IR
- RSB

USB 2.0 DRD

- Support AMBA AHB Slave mode
- Support the Host Negotiation Protocol (HNP) and the Session Request Protocol (SRP)
- Support the UTMI+ Level 3 interface . The 8-bit bidirectional data buses are used.
- 64-Byte Endpoint 0 for Control Transfer (Endpoint0)
- Support High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Support point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Include automatic ping capabilities
- Soft connect/disconnect function
- Perform all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Include interface to an external Dedicated Central DMA controller. Data is transferred through Special bus for saving ABH bus bandwidth
- Support industry-standard single port SRAM for USB Configurable Data FIFO. The size is 2048 byte with 32-bit word width. The RAM can be used by other modules when USB/DRD disable

KEYADC

- 6-bit resolution
- Support hold key and general key
- Support single key and continuous key
- Sample rate up to 250Hz

TP

- 12-bit SAR type A/D converter
- 4-wire I/F
- Dual Touch Detect
- Touch-pressure measurement
- Sampling frequency: 2MHz
- Single-Ended conversion of touch screen inputs and ratio metric conversion of touch screen inputs
- TACQ up to 262ms
- Median and averaging filter to reduce noise
- Pen down detection, with programmable sensitivity
- Support X, Y change function

Digital Audio Interface

- I2S or PCM configured by software
- Master / Slave Mode operation configured by software
- I2S Audio data sample rate from 8Khz to 192Khz
- I2S Data format for standard I2S, Left Justified and Right Justified
- PCM supports linear sample (8-bits or 16-bits), 8-bits u-law and A-law commanded sample

UART

- Compatible with industry-standard 16550 UARTs
- 32-Bytes Transmit and receive data FIFOs
- DMA controller interface
- Software/ Hardware Flow Control

- Programmable Transmit Holding Register Empty interrupt
- Support IrDa 1.0 SIR
- Interrupt support for FIFOs, Status Change

SPI

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four chip selects to support multiple peripherals for SPI0 and SPI1 has one chip select
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the chip select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

TWI

- Software-programmable for Slave or Master
- Support repeated START signal
- Multi-master systems supported
- Allow 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and general call address detection
- Interrupt on address detection
- Support speeds up to 400Kbits/s (‘fast mode’)
- Allow operation from a wide range of input clock frequencies

IR

- Support APB 16-bits bus width
- Full physical layer implementation
- Support CIR for remote control
- 64x8bits FIFO for data buffer
- Programmable FIFO thresholds

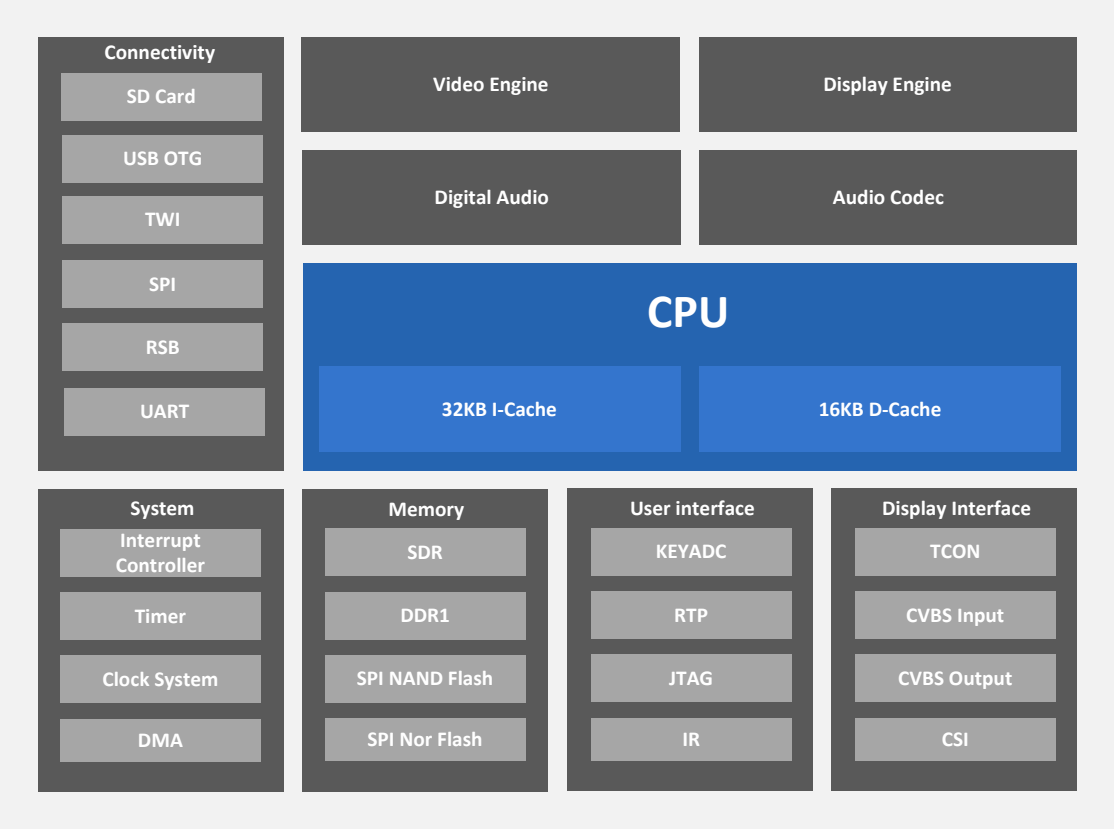
RSB

- Support speed up to 20MHz with ultra low power
- Support push-pull bus
- Support host mode
- Support programmable output delay of CD signal
- Support parity check for address and data transmission
- Support multi-devices

2.9. Process and Package

- Package eLQFP128

3. Block Diagram



4. Pin Description

4.1. Pin Characteristics

Following table describes the F1C500 pin characteristics from seven aspects: ***BALL#, Pin Name, Default Function[1], Type[2], Reset*** State[3], Default Pull Up/Down[4], and Buffer Strength[5].

Pin Num	Pin Name	Default Function	Type	Reset State	Default Pull Up/ Down	Buffer Strength (mA)
SDRAM						
25	DA3	DRAM	O	Z	-	-
26	DA2	DRAM	O	Z	-	-
27	DA1	DRAM	O	Z	-	-
28	DA0	DRAM	O	Z	-	-
29	DA10	DRAM	O	Z	-	-
30	BA1	DRAM	O	Z	-	-
31	BA0	DRAM	O	Z	-	-
32	DRAMVCC	DRAM	P	Z	-	-
33	RAS	DRAM	O	Z	-	-
34	CAS	DRAM	O	Z	-	-
36	DQM0	DRAM	O	Z	-	-
35	SWE	DRAM	O	Z	-	-
37	DQ0	DRAM	I/O	H	pull-up	-
38	DQ1	DRAM	I/O	H	pull-up	-
39	DQ2	DRAM	I/O	H	pull-up	-
40	DQ3	DRAM	I/O	H	pull-up	-
41	DQ4	DRAM	I/O	H	pull-up	-
42	DQ5	DRAM	I/O	H	pull-up	-
43	DQ6	DRAM	I/O	H	pull-up	-
44	DQ7	DRAM	I/O	H	pull-up	-
45	DQS0	DRAM	I/O	H	pull-up	-
46	DRAMVCC	DRAM	P	-	-	-
47	DRAMVREF	DRAM	P	-	-	-
48	DQS1	DRAM	I/O	H	pull-up	-
49	DQ8	DRAM	I/O	H	pull-up	-
50	DQ9	DRAM	I/O	H	pull-up	-
51	DQ10	DRAM	I/O	H	pull-up	-
52	DQ11	DRAM	I/O	H	pull-up	-
53	DQ12	DRAM	I/O	H	pull-up	-
54	DQ13	DRAM	I/O	H	pull-up	-
55	DQ14	DRAM	I/O	H	pull-up	-
57	DQ15	DRAM	I/O	H	pull-up	-
58	DQM1	DRAM	O	Z	-	-
59	DRAMVCC	DRAM	P	-	-	-

60	CKB	DRAM	O	Z	-	-
61	CK	DRAM	O	Z	-	-
62	CKE	DRAM	O	Z	-	-
63	DA12	DRAM	O	Z	-	-
64	DA11	DRAM	O	Z	-	-
66	DA8	DRAM	O	Z	-	-
65	DA9	DRAM	O	Z	-	-
67	DA7	DRAM	O	Z	-	-
68	DA6	DRAM	O	Z	-	-
69	DA5	DRAM	O	Z	-	-
70	DA4	DRAM	O	Z	-	-
GPIOC						
93	PC0	GPIO	I/O	Disabled	-	-
94	PC1	GPIO	I/O	Disabled	pull-up	-
95	PC2	GPIO	I/O	Disabled	-	-
96	PC3	GPIO	I/O	Disabled	-	-
GPIOD						
1	PD0	GPIO	I/O	Disabled	-	-
2	PD1	GPIO	I/O	Disabled	-	-
3	PD2	GPIO	I/O	Disabled	-	-
4	PD3	GPIO	I/O	Disabled	-	-
5	PD4	GPIO	I/O	Disabled	-	-
6	PD5	GPIO	I/O	Disabled	-	-
7	PD6	GPIO	I/O	Disabled	-	-
8	PD7	GPIO	I/O	Disabled	-	-
9	PD8	GPIO	I/O	Disabled	-	-
10	PD9	GPIO	I/O	Disabled	-	-
11	PD10	GPIO	I/O	Disabled	-	-
12	PD11	GPIO	I/O	Disabled	-	-
13	PD12	GPIO	I/O	Disabled	-	-
14	PD13	GPIO	I/O	Disabled	-	-
16	PD14	GPIO	I/O	Disabled	-	-
17	PD15	GPIO	I/O	Disabled	-	-
18	PD16	GPIO	I/O	Disabled	-	-
19	PD17	GPIO	I/O	Disabled	-	-
20	PD18	GPIO	I/O	Disabled	-	-
21	PD19	GPIO	I/O	Disabled	-	-
22	PD20	GPIO	I/O	Disabled	-	-
24	PD21	GPIO	I/O	Disabled	-	-
GPIOE						
83	PE0	GPIO	I/O	Disabled	-	-
82	PE1	GPIO	I/O	Disabled	-	-
81	PE2	GPIO	I/O	Disabled	-	-
80	PE3	GPIO	I/O	Disabled	-	-
79	PE4	GPIO	I/O	Disabled	-	-
78	PE5	GPIO	I/O	Disabled	-	-
77	PE6	GPIO	I/O	Disabled	-	-

76	PE7	GPIO	I/O	Disabled	-	-
75	PE8	GPIO	I/O	Disabled	-	-
74	PE9	GPIO	I/O	Disabled	-	-
73	PE10	GPIO	I/O	Disabled	-	-
72	PE11	GPIO	I/O	Disabled	-	-
71	PE12	GPIO	I/O	Disabled	-	-
GPIOF						
92	PF0	GPIO	I/O	Disabled	-	-
91	PF1	GPIO	I/O	Disabled	-	-
90	PF2	GPIO	I/O	Disabled	-	-
89	PF3	GPIO	I/O	Disabled	-	-
88	PF4	GPIO	I/O	Disabled	-	-
87	PF5	GPIO	I/O	Disabled	-	-
USB						
101	UVCC	-	P	-	-	-
103	DP	-	A	-	-	-
102	DM	-	A	-	-	-
Audio Codec						
116	VRA1	-	A	-	-	-
118	VRA2	-	A	-	-	-
117	AGND	-	P	-	-	-
119	FMINR	-	A	-	-	-
120	FMINL	-	A	-	-	-
121	MICIN	-	A	-	-	-
122	LINL	-	A	-	-	-
123	HPR	-	A	-	-	-
124	HPL	-	A	-	-	-
125	HPCOM	-	A	-	-	-
127	HPVCC	-	P	-	-	-
126	HPCOM_FB	-	A	-	-	-
115	AVCC	-	P	-	-	-
Touch Panel						
100	TP_X1	-	A	-	-	-
98	TP_X2	-	A	-	-	-
99	TP_Y1	-	A	-	-	-
97	TP_Y2	-	A	-	-	-
TV IN						
108	TVAVCC	-	P	-	-	-
109	TVGND	-	P	-	-	-
110	TV_VRN	-	A	-	-	-
111	TV_VRP	-	A	-	-	-
112	TVIN1	-	A	-	-	-
113	TVIN0	-	A	-	-	-
KEYADC						
114	KEYADCIN	-	A	-	-	-
TV OUT						
107	TVOUT	-	A	-	-	-

Clock						
85	OSC24MO	-	A	-	-	-
86	OSC24MI	-	A	-	-	-
Miscellaneous Signal						
104	NMI	-	I	-	-	-
105	RESET	-	I	-	-	-
Power						
128	VCC	-	P	-	-	-
15	VCC	-	P	-	-	-
84	VCC	-	P	-	-	-
23	VDD	-	P	-	-	-
56	VDD	-	P	-	-	-
106	VDD	-	P	-	-	-
	GND	-	G	-	-	-

Note:

1 ***Default function*** defines the default function of each pin, especially for pins with multiplexing functions;

2 There are five ***pin types*** here: O for output, I for input, I/O for input/output, A for analog,OD for Open-Drain, P for power and G for ground;

3 ***Reset state*** defines the state of the terminal at reset: Z for high-impedance.

4 ***Default Pull up/down*** defines the presence of an internal pull up or pull down resistor. Unless otherwise specified, the pin is default to be floating, and can be configured as pull up or pull down;

5 ***Buffer strength*** defines the driver strength of the associated output buffer. It is tested in the condition that VCC= 3.0V, strength=MAX;

4.2. GPIO Multiplexing Functions

Following table provides a description of the GPIO multiplexing functions of F1C500.

Port	Default Function	IO Type	Default IO State	Default Pull-up/ down	Multiplexing Function 2	Multiplexing Function 3	Multiplexing Function 4	Multiplexing Function 5	Multiplexing Function 6
PC0	GPIO	I/O	DIS	Z	SPI0_CLK	SDC1_CLK			
PC1	GPIO	I/O	DIS	Z	SPI0_CS	SDC1_CMD			
PC2	GPIO	I/O	DIS	Z	SPI0_MISO	SDC1_D0			
PC3	GPIO	I/O	DIS	Z	SPI0_MOSI	UART0_TX			
PD0	GPIO	I/O	DIS	Z	LCD_D2	TWI0_SDA	RSB_SDA		EINTD0
PD1	GPIO	I/O	DIS	Z	LCD_D3	UART1_RTS			EINTD1
PD2	GPIO	I/O	DIS	Z	LCD_D4	UART1_CTS			EINTD2
PD3	GPIO	I/O	DIS	Z	LCD_D5	UART1_RX			EINTD3
PD4	GPIO	I/O	DIS	Z	LCD_D6	UART1_TX			EINTD4
PD5	GPIO	I/O	DIS	Z	LCD_D7	TWI1_SCK			EINTD5
PD6	GPIO	I/O	DIS	Z	LCD_D10	TWI1_SDA			EINTD6
PD7	GPIO	I/O	DIS	Z	LCD_D11	DA_MCLK			EINTD7
PD8	GPIO	I/O	DIS	Z	LCD_D12	DA_BCLK			EINTD8
PD9	GPIO	I/O	DIS	Z	LCD_D13	DA_LRCK			EINTD9
PD10	GPIO	I/O	DIS	Z	LCD_D14	DA_IN			EINTD10

PD11	GPIO	I/O	DIS	Z	LCD_D15	DA_OUT			EINTD11
PD12	GPIO	I/O	DIS	Z	LCD_D18	TWI0_SCK	RSB_SCK		EINTD12
PD13	GPIO	I/O	DIS	Z	LCD_D19	UART2_TX			EINTD13
PD14	GPIO	I/O	DIS	Z	LCD_D20	UART2_RX			EINTD14
PD15	GPIO	I/O	DIS	Z	LCD_D21	UART2_RTS	TWI2_SCK		EINTD15
PD16	GPIO	I/O	DIS	Z	LCD_D22	UART2_CTS	TWI2_SDA		EINTD16
PD17	GPIO	I/O	DIS	Z	LCD_D23	OWA_OUT			EINTD17
PD18	GPIO	I/O	DIS	Z	LCD_CLK	SPI0_CS			EINTD18
PD19	GPIO	I/O	DIS	Z	LCD_DE	SPI0_MOSI			EINTD19
PD20	GPIO	I/O	DIS	Z	LCD_HSYNC	SPI0_CLK			EINTD20
PD21	GPIO	I/O	DIS	Z	LCD_VSYNC	SPI0_MISO			EINTD21
PE0	GPIO	I/O	DIS	Z	CSI_HSYNC	LCD_D0	TWI2_SCK	UART0_RX	EINTE0
PE1	GPIO	I/O	DIS	Z	CSI_VSYNC	LCD_D1	TWI2_SDA	UART0_TX	EINTE1
PE2	GPIO	I/O	DIS	Z	CSI_PCLK	LCD_D8	CLK_OUT		EINTE2
PE3	GPIO	I/O	DIS	Z	CSI_D0	LCD_D9	DA_BCLK	RSB_SCK	EINTE3
PE4	GPIO	I/O	DIS	Z	CSI_D1	LCD_D16	DA_LRCK	RSB_SDA	EINTE4
PE5	GPIO	I/O	DIS	Z	CSI_D2	LCD_D17	DA_IN		EINTE5
PE6	GPIO	I/O	DIS	Z	CSI_D3	PWM1	DA_OUT	OWA_OUT	EINTE6
PE7	GPIO	I/O	DIS	Z	CSI_D4	UART2_TX	SPI1_CS		EINTE7
PE8	GPIO	I/O	DIS	Z	CSI_D5	UART2_RX	SPI1_MOSI		EINTE8
PE9	GPIO	I/O	DIS	Z	CSI_D6	UART2_RTS	SPI1_CLK		EINTE9
PE10	GPIO	I/O	DIS	Z	CSI_D7	UART2_CTS	SPI1_MISO		EINTE10
PE11	GPIO	I/O	DIS	Z	CLK_OUT	TWI0_SCK	IR_RX		EINTE11
PE12	GPIO	I/O	DIS	Z	DA_MCLK	TWI0_SDA	PWM0		EINTE12
PF0	GPIO	I/O	DIS	Z	SDC0_D1	DBG_MS	IR_RX		EINTF0
PF1	GPIO	I/O	DIS	Z	SDC0_D0	DBG_DI			EINTF1
PF2	GPIO	I/O	DIS	Z	SDC0_CLK	UART0_RX			EINTF2
PF3	GPIO	I/O	DIS	Z	SDC0_CMD	DBG_DO			EINTF3
PF4	GPIO	I/O	DIS	Z	SDC0_D3	UART0_TX			EINTF4
PF5	GPIO	I/O	DIS	Z	SDC0_D2	DBG_CK	PWM1		EINTF5

4.3. Detailed Pin Description

Pin Name	Description	Type
SDRAM		
DQ[15:0]	DRAM Data Bus Bit [15:0]	I/O
DQM0	DRAM Input Data Mask for DQ0~DQ7	O
DQM1	DRAM Input Data Mask for DQ8~DQ15	O
CK	DRAM (Positive) Clock	O
CKE	DRAM Clock Enable	O
DA[12:0]	DRAM Address Bit [12:0]	O
SWE	DRAM Write Enable	O
RAS	DRAM Row Address Strobe	O
CAS	DRAM Column Address Strobe	O
BA[1:0]	DRAM Bank Address [1:0]	O

DQS0	DRAM Data Strobe for DQ0~DQ7	I/O
DQS1	DRAM Data Strobe for DQ8~DQ15	I/O
CKB	DRAM (Negative) Clock	O
DRAMVREF	DRAM Reference Voltage	P
DRAMVCC	DRAM Power Supply	P
GPIO		
PC[4:0]	Port C Bit[4:0]	I/O
PD[21:0]	Port D Bit[21:0]	I/O
PE[12:0]	Port E Bit[12:0]	I/O
PF[5:0]	Port F Bit[5:0]	I/O
USB		
USBDM	USB DM signal	-
USBDP	USB DP signal	-
UVCC	USB 3.3V power	-
Audio Codec		
HPOUTL	Headphone Left output	-
HPOUTR	Headphone Right output	-
HPCOM	Headphone common reference	-
HPCOMFB	Headphone common reference feedback	-
HPVCC	Headphone Amplifier Power	-
FMINL	FM in Left input	-
FMINR	FM in Right input	-
LINEIN	Line in input	-
MICIN	Microphone input	-
VRA1	Reference	-
VRA2	Reference	-
AVCC	Analog Power	-
AGND	Analog Ground	-
Digital Audio		
DA_MCLK	Digital Audio Master Clock	I/O
DA_BCLK	Digital Audio Bit Clock	I/O
DA_LRCK	Digital Audio Left & Right channel Clock	I/O
DA_IN	Digital Audio Data Out	I/O
DA_OUT	Digital Audio Data in	I/O
RSB		
RSB_SCK	RSB Clock	I/O
RSB_SDA	RSB Data	I/O
Touch Panel		
TP_X1	Touch Panel X1 input	-
TP_X2	Touch Panel X2 input	-
TP_Y1	Touch Panel Y1 input	-

TP_Y2	Touch Panel Y1 input	-
TV-Out		
TVOUT	TV CVBS Output	-
TV-IN		
TVIN0	TV CVBS Input 0	-
TVIN1	TV CVBS Input 1	-
TVAVCC	TV Analog VCC for TVIN and TVOUT	-
TVAGND	TV Analog GND for TVIN and TVOUT	-
TVIN_VRP	TV Input Voltage Reference Positive	-
TVIN_VRN	TV Input Voltage Reference Negative	-
Clock		
OSC24MI	24MHz Crystal Input	-
OSC24MO	24MHz Crystal Output	-
Miscellaneous Signal		
NMI#	Not Mask Interrupt Input	I
RESET#	Chip Reset Signal	I
PWM[1:0]	PWM	I/O
KEYADC		
KEYADC0	ADC input for key	-
LCD		
LCD[23:0]	LCD Data Bus Bit[23:0]	I/O
LCDCLK	LCD Clock	I/O
LCDDE	LCD Data Enable	I/O
LCDHSYNC	LCD Horizon Sync	I/O
LCDVSYNC	LCD Vertical Sync	I/O
SPI(x=[1:0])		
SPIx_MOSI	SPI Master Output Slave Input	I/O
SPIx_MISO	SPI Master Input Slave Output	I/O
SPIx_CS	SPI Chip Select Signal	I/O
SPIx_CLK	SPI Clock	I/O
UART(x=[2:0])		
UARTx_TX	UART Data Transmit	I/O
UARTx_RX	UART Data Receive	I/O
UARTx_CTS	UART Clear To Send	I/O
UARTx_RTS	UART Request To Send	I/O
IR		
IR_TX	IR Transmit Signal	I/O
IR_RX	IR Receive Signal	I/O
CSI		
CSI-PCLK	CSI Pixel Clock Output signal	I/O
CSI-HSYNC	CSI Horizontal Synchronization signal	I/O

CSI-VSYNC	CSI Vertical Synchronization signal	I/O
CSI-D[7:0]	CSI Data Bit[7:0]	I/O
SDC0		
SDC0_D[3:0]	SCD/MMC/SDIO Data Bit[3:0]	I/O
SDC0_CLK	SCD/MMC/SDIO Clock	I/O
SDC0_CMD	SCD/MMC/SDIO Command	I/O
SDC1		
SDC1_D0	SCD/MMC/SDIO Data Bit0	I/O
SDC1_CLK	SCD/MMC/SDIO Clock	I/O
SDC1_CMD	SCD/MMC/SDIO Command	I/O
TWI(x=[2:0])(Open-Drain)		
TWIx-SCK	TWI Clock	I/O
TWIx-SDA	TWI Data	I/O
POWER		
VDD	Core VDD 1.2V power	-
VCC	IO VCC 3.3V Power	-

5.Electrical Characteristics

5.1. Absolute Maximum Ratings

Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

SYMBOL	PARAMETER		MIN	MAX	UNIT
T_g	Storage Temperature		-65	150	℃
$I_{I/O}$	In/Out current for input and output		-	-	mA
V_{ESD}	ESD stress voltage	HBM(human body model)	-	-	V_{ESD}
		CDM(charged device model)	NA	NA	
T_J	Junction Temperature		-	125	℃
VCC	Power Supply for I/O		-0.3	3.6	V
AVCC	Power Supply for Codec		-0.3	3.1	V
TVAVCC	Power Supply for TV		-0.3	3.6	V
VDD	Power Supply for Internal Digital Logic		-0.3	1.3	V
UVCC	Power Supply for USB		-0.3	3.6	V
DRAMVCC	Power Supply for DDR1		-0.3	2.7	V
	Power Supply for SDR		-0.3	3.6	V

5.2. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX
T_a	Ambient Operating Temperature[Commercial]	-20	-	85
	Operating Temperature[Extended]	NA	NA	NA
VCC	Power Supply for I/O	3.0	3.3	3.6
AVCC	Power Supply for Codec	2.5	2.8	3.1
TVAVCC	Power Supply for TV	3.0	3.3	3.6
VDD	Power Supply for Internal Digital Logic	1.0	1.1	1.2
UVCC	Power Supply for USB	3.0	3.3	3.6
DRAMVCC	Power Supply for DDR1	2.3	2.5	3.7
DRAMVCC	Power Supply for SDR	3.0	3.3	3.6

5.3. DC Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-Level Input Voltage	VCC-IO[1]=3.0V	2.1	-	3.6	V
		VCC-IO = 1.8V	1.1	-	1.98	V
V_{IL}	Low-Level Input Voltage	VCC-IO=3.0V	-0.3	-	0.7	V
		VCC-IO = 1.8V	-0.3	-	0.7	V
V_{HYS}	Hysteresis Voltage	-	-	-	-	mV
I_{IH}	High-Level Input Current	VCC-IO=3.0V, VI=3.0V	TBD	TBD	TBD	uA
		VCC-IO = 1.8V	TBD	TBD	TBD	uA
I_{IL}	Low-Level Input Current	VCC-IO=3.0V, VI=0V	TBD	TBD	TBD	uA
		VCC-IO = 1.8V	TBD	TBD	TBD	uA
V_{OH}	High-Level Output Voltage	VCC-IO=3.0V	2.7	-	NA	V
		VCC-IO = 1.8V	1.5	-	NA	V
V_{OL}	Low-Level Output Voltage	VCC-IO=3.0V	NA	-	0.4	V
		VCC-IO = 1.8V	NA	-	0.4	V
I_{OZ}	Tri-State Output Leakage Current	VCC-IO=3.0V	TBD	TBD	TBD	uA
		VCC-IO = 1.8V	TBD	TBD	TBD	uA
C_{IN}	Input Capacitance	-	NA	NA	5	pF
C_{OUT}	Output Capacitance	-	NA	NA	5	pF

5.4. Oscillator Electrical Characteristics

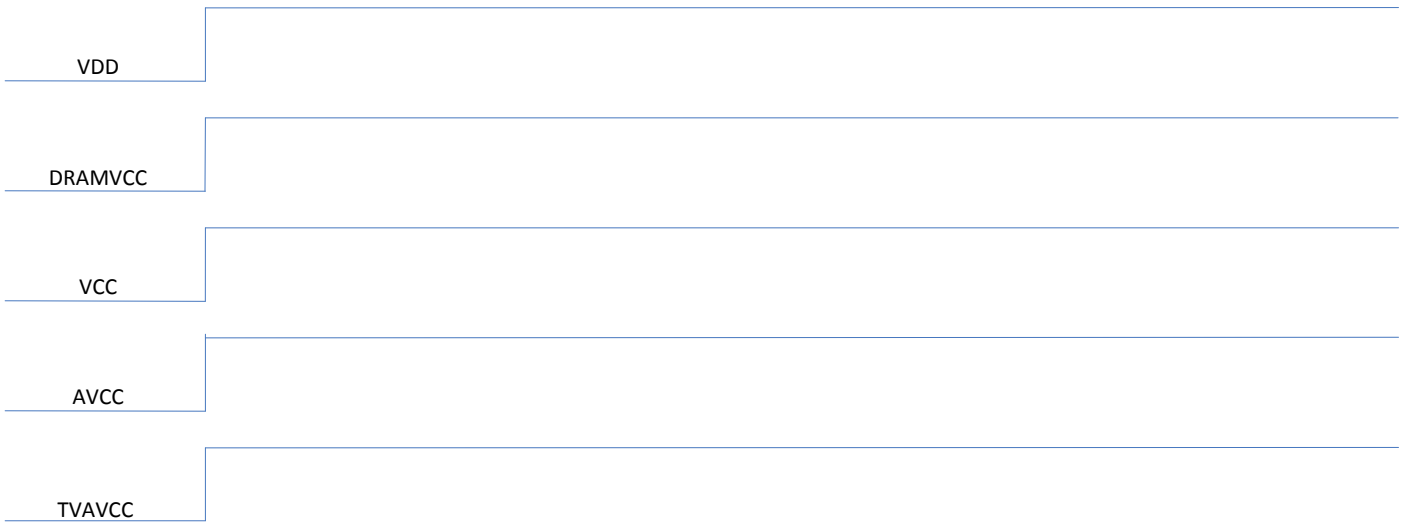
The F1C500 contains a 24MHz oscillator.
The 24MHz crystal is connected between the OSC24MI and OSC24MO.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
1/(tCPMAIN)	Crystal Oscillator Frequency Range	-	24	-	MHz
t_{ST}	Startup Time	-	-	-	ms
	Frequency Tolerance at 25°C	-50	-	50	ppm
	Oscillation Mode	Fundamental		-	
	Maximum Change Over Temperature Range	-50	-	50	ppm
PON	Drive Level	-	-	50	uW
CL	Equivalent Load Capacitance	-	-	-	pF
CL1,CL2	Internal Load Capacitance(CL1=CL2)	-	-	-	pF
RS	Series Resistance(ESR)	-	-	-	Ω
	Duty Cycle	30	50	70	%
CM	Motional Capacitance	-	-	-	pF
C_{SHUT}	Shunt Capacitance	-	-	-	pF
R_{BIAS}	Internal Bias Resistor	-	-	-	MΩ

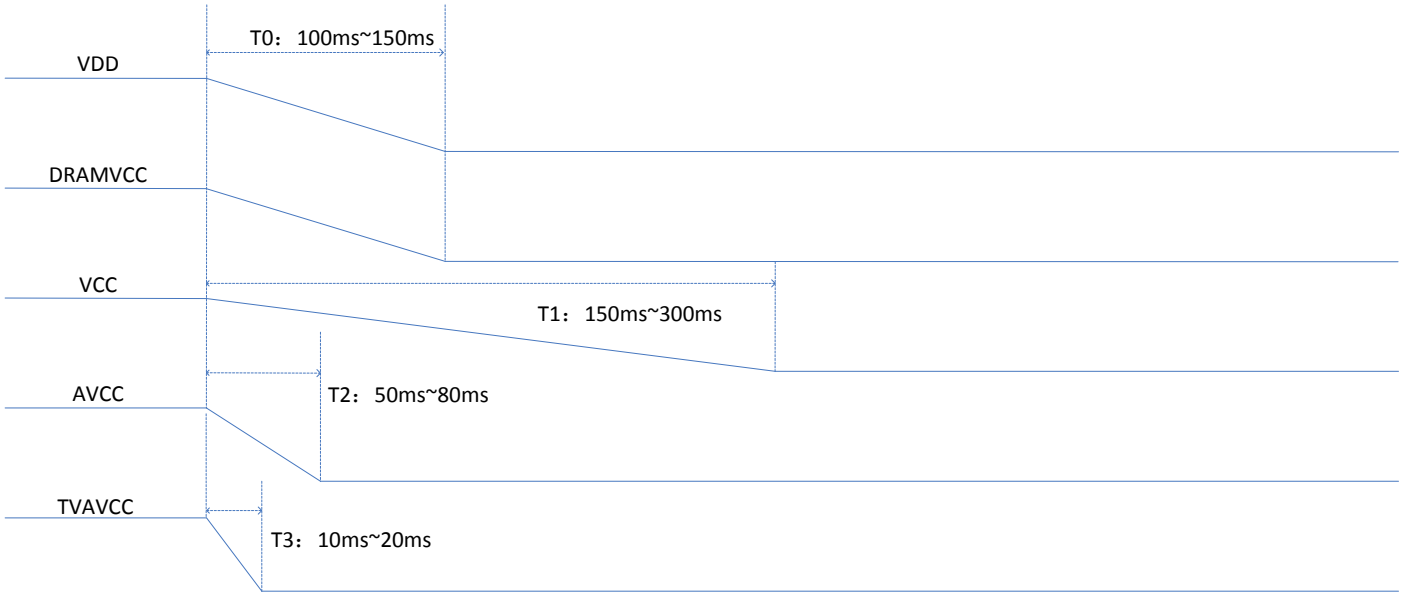
5.5. Power Up/Down Sequence

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operations.

Power On Sequence

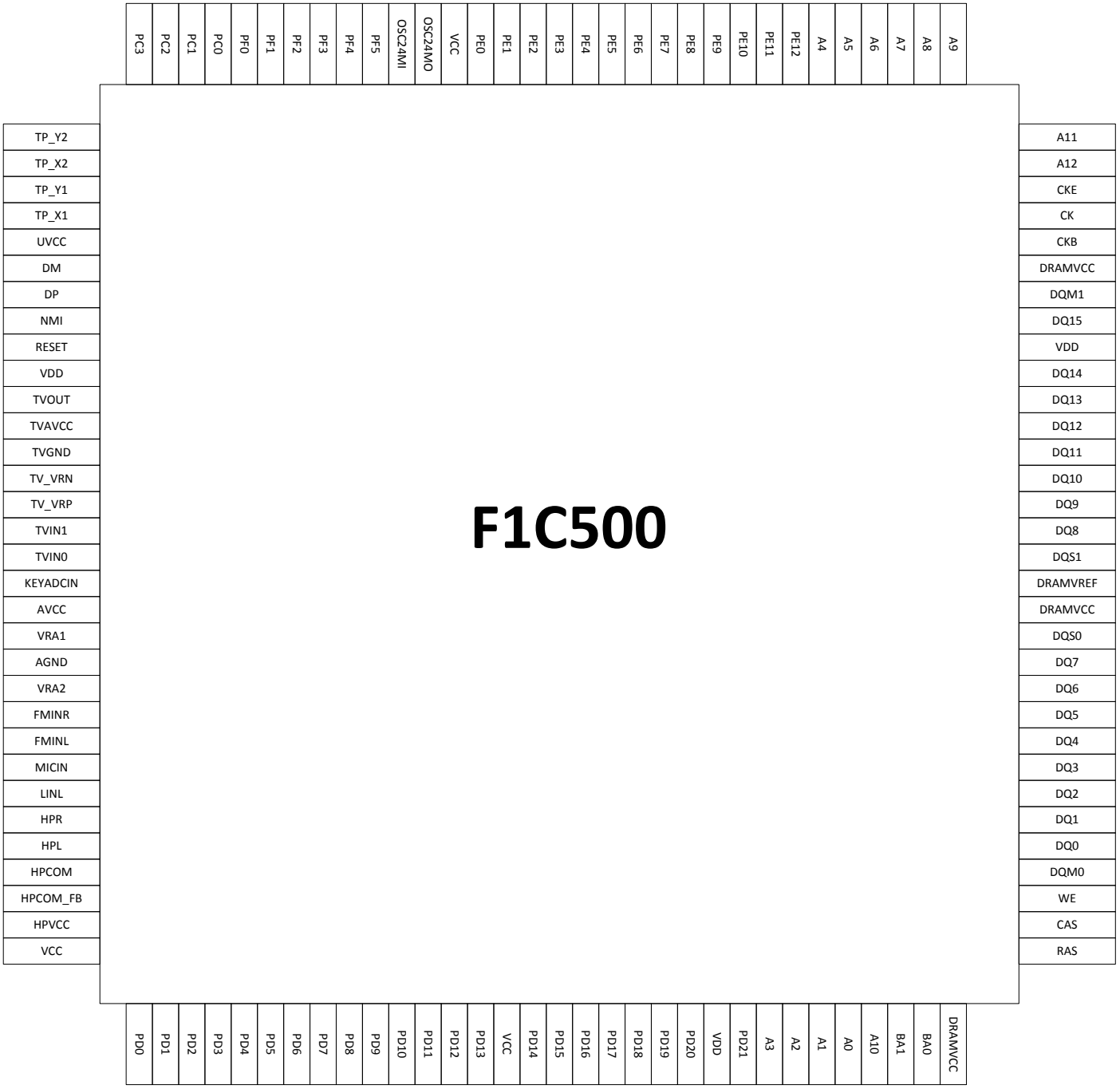


Power Down Sequence

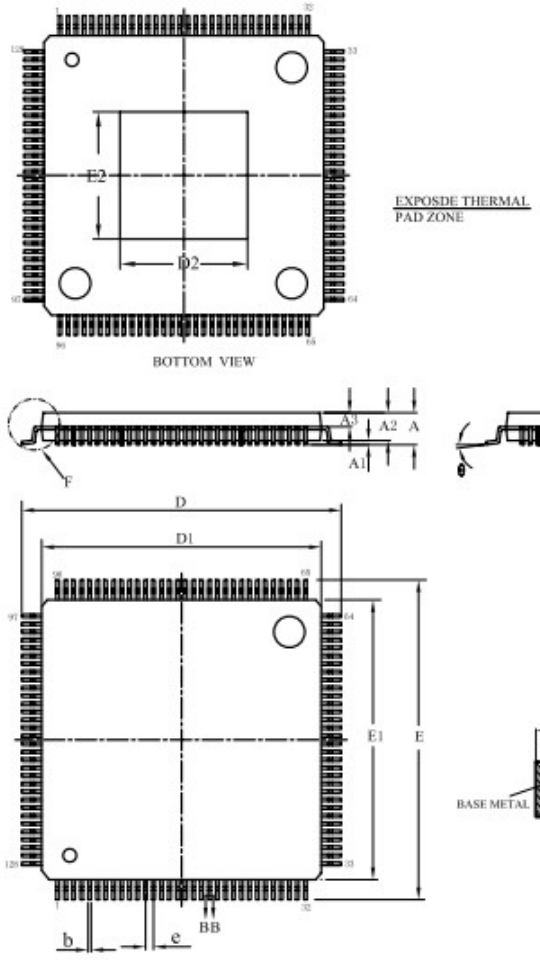


6. Pin Assignment

6.1. Pin Map



6.2. Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.15	—	0.23
b1	0.14	0.16	0.19
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	—	15.35
e	0.40BSC		
L	0.45	—	0.75
L1	1.00BSC		
θ	0		8°

	D2	E2
300*300	6.88REF	6.88REF
218*218	4.95REF	4.95REF
200*286	5.08REF	7.26REF
230*275	5.60REF	6.75REF